

FORM PTO 1449 ( <i>modified</i> )  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  LIST OF REFERENCES CITED BY APPLICANT(S) (Use several sheets if necessary)				ATTY DOCKET NO. <b>NL031031US1</b>		APPLICATION NO. <b>10/570,290</b>	
				APPLICANT <b>Adrianus Josephus Bink, et al.</b>			
				FILING DATE <b>February 28, 2008</b>		GROUP <b>2185</b>	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		<b>5,666,482</b>	<b>9/9/1997</b>	<b>McClure</b>			
		<b>5,958,068</b>	<b>9/28/1999</b>	<b>Arimilli, et al.</b>			
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FOREIGN PATENT DOCUMENTS							
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OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)							
		<b>Yamashita, K. et al. "A Design and Yield Evaluation Technique for Wafer-Scale Memory", Computer, vol. 25, issue 4, pgs. 19-27 (4/1992)</b>					
		<b>Otterstedt, et al. "Test and Reconfiguration Experiments for a Defect-Tolerant Large Area Monolithic Multiprocessor System", Proc. of Int. Conf. on Wafer Scale Integration, San Francisco, pp. 315-23 (1/1994)</b>					
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		<b>Shirvani, et al. "PADded Cache: A New Fault-Tolerance Technique for Cache Memories", Proc. 17th IEEE VLSI Test Symposium (1999)</b>					
		<b>Chakraborty, K. et al. "A Physical Design Tool for Build-In Self-Repairable Static Rams", Proc. of the Conf. on Design, Automation, and Test in Europe, Munich, DE (1999)</b>					
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		<b>Baik, et al. "Re-evaluation and Comparison of Fault Tolerant Cache Schemes", Univ. of Wisconsin Madison ECE Dept. 753 Course Project (2002)</b>					
		<b>International Preliminary Report on Patentability for Int'l. Patent Appln. No. PCT/IB2004/51465 (March 6, 2006)</b>					
EXAMINER				DATE CONSIDERED			

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.